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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/936,041	12/18/2001	Ichio Yudasaka	110553	7809

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EXAMINER	
ROMAN, ANGEL	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 07/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/936,041	Applicant(s) YUDASAKA ET AL.	
	Examiner Angel Roman	Art Unit 2812	

-- The MAILING DATE of this communicati n appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *16-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim U.S. Patent 6,355,510 B1 in view of Wang et al. U.S. Patent 6,171,913 B1.

Kim discloses a method of manufacturing a thin film transistor by forming a channel region 25c facing a gate electrode 27 through a gate insulating film 26; forming source and drain regions (25S, 25D) connected to the channel region in a

semiconductor film 25 that is formed on a surface of an insulating substrate 24. The semiconductor film 25 is formed by recrystallizing an amorphous silicon film using a laser annealing method (see column 3, lines 47-50). The impurity regions forming the source and drain may be formed before forming the gate region and after recrystallizing the semiconductor film 25 (see figures 3A-3B).

Kim is applied as above but lacks anticipation on forming a recombination center by introducing an impurity by injecting the impurity from a surface side of said channel region so that a distance between the recombination center and the drain region is shorter than a distance between the recombination center and the source region, wherein the recombination center is detached from the drain region and said impurity being at least one kind selected from the group including inert gases, metals, Group III elements, Group IV elements and Group V elements, the process of introducing said impurity into said channel region being carried out, before or after said gate insulating film and said gate electrode are sequentially formed on an surface side of said channel region, injecting the impurity from a surface side of said gate electrode before an interlayer insulating film is formed on a surface side of the gate electrode wherein an average projected range of the impurity in said process of, introducing an impurity being from a center in a direction of thickness of said channel region to an interface between the channel region and the gate insulating film and the distance from the recombination center to the drain region and the distance from the recombination center to the source region are in the range of 1/10 to 1/3 of the channel length; introducing said impurity to said channel region in a crystallization process by impurity diffusion from an impurity

diffusion source arranged at a lower layer side of said channel region; disclosing maximum process temperatures of 300 degrees Celsius; and disclosing that the transistor is use in a display device.

With respect to forming a recombination center by introducing an impurity by injecting the impurity from a surface side of said channel region so that a distance between the recombination center and the drain region is shorter than a distance between the recombination center and the source region, wherein the recombination center is detached from the drain region and said impurity being at least one kind selected from the group including inert gases, metals, Group III elements, Group IV elements and Group V elements, the process of introducing said impurity into said channel region being carried out, before or after said gate insulating film and said gate electrode are sequentially formed on an surface side of said channel region, by injecting the impurity from a surface side of said gate electrode before an interlayer insulating film is formed on a surface side of the gate electrode wherein an average projected range of the impurity in said process of, introducing an impurity from a center in a direction of thickness of said channel region to an interface between the channel region and the gate insulating film and the distance from the recombination center to the drain region and the distance from the recombination center to the source region are in the range of 1/10 to 1/3 of the channel length; Wang et al. discloses a method of manufacturing a thin film transistor by forming a channel region facing a gate electrode 8 through a gate insulating film 9; forming source and drain regions (26, 27) connected to the channel region in a semiconductor film; and forming a recombination center 33 by

introducing an impurity by injecting the impurity from a surface side of said channel region so that a distance between the recombination center 33 and the drain region 27 is shorter than a distance between the recombination center 33 and the source region 26, wherein the recombination center 33 is detached from the drain region 27 and said impurity is one kind selected from the group including inert gases, metals, Group III elements, Group IV elements and Group V elements; the process of introducing said impurity into said channel region is carried out, after said gate insulating film and said gate electrode are sequentially formed on an surface side of said channel region, by injecting the impurity from a surface side of said gate electrode before an interlayer insulating film is formed on a surface side of the gate electrode wherein an average projected range of the impurity in said process of, introducing an impurity being from a center in a direction of thickness of said channel region to an interface between the channel region and the gate insulating film and the distance from the recombination center to the drain region and the distance from the recombination center to the source region are in the range of 1/10 to 1/3 of the channel length (see figure 3). In view of this disclosure, it would have been obvious to a person having ordinary skills in the art at the time the invention was made to form a recombination center in the channel region of the transistor disclosed in the primary reference of Kim using the method disclosed by Wang et al. by forming the recombination center before or after the gate insulating film and the gate electrode are formed since it would improve low puchthrough resistance (see Wang et al. column 1, lines 11-33); forming the recombination center before the gate insulating film and the gate are formed lacks any criticality and it is an obvious

alternate method of introducing impurities into semiconductor regions (see Kim figure 3A), therefore it would also have been obvious to formed the recombination center before the gate insulating layer and the gate are formed in the primary reference of Kim as modified by Wang et al..

Regarding introducing said impurity to said channel region in a crystallization process by impurity diffusion from an impurity diffusion source arranged at a lower layer side of said channel region, it would have been obvious to a person having ordinary skills in the art at the time the invention was made to introduce said impurity to said channel region by impurity diffusion from an impurity diffusion source arranged at a lower layer side of said channel region in a crystallization process on a semiconductor film in the primary reference of Kim as modified by Wang et al. since diffusing an impurity by diffusing from an impurity diffusion source arranged at a lower layer side of a channel region during a crystallization process of a semiconductor film is an alternate conventional method of introducing an impurity, and is only considered to be an optimum process of introducing an impurity by performing routine experimentation based on a desire accuracy and manufacturing costs.

With respect to process temperatures after introducing said impurities to said channel region being less than 300 °C, selecting an optimum maximum temperature of less than 300 °C for subsequent processes in the primary reference of Kim as modified by Wang et al. would have been obvious to a person having ordinary skills in the art at the time the invention was made since selecting process temperatures of less than 300 °C is only considered to be routine optimization, furthermore there is no indication of

using process temperatures higher than 300 °C in subsequent processes in the primary reference of Kim as modified by Wang et al..

Regarding using the transistor in a display device, this limitation is only considered to be an intended use of the device being manufacture since it is well known in the art to use transistors in display devices therefore this limitation has not being given patentable weight.

Response to Arguments

4. Applicant's arguments with respect to claims 1-15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yudasaka et al. and Lin et al. disclose methods of forming recombination centers close to drain regions in thin film transistors.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel Roman whose telephone number is (703) 306-0207. The examiner can normally be reached on Monday-Friday 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers

for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

AR
June 26, 2003

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800